

NCV8402

Self-Protected Low Side Driver with Temperature and Current Limit

NCV8402 is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

Features

- Short-Circuit Protection
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- RoHs Compliant
- AEC-Q101 Qualified
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- These are Pb-Free Devices

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

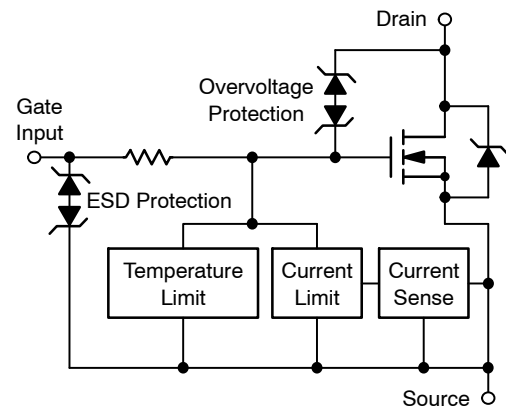


ON Semiconductor®

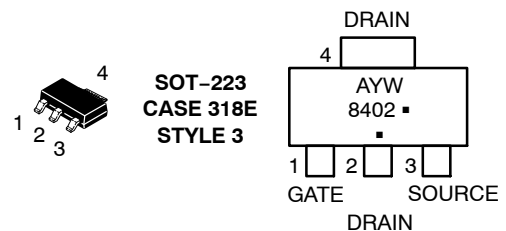
<http://onsemi.com>

| $V_{(BR)DSS}$ (Clamped) | $R_{DS(ON)}$ TYP | I_D MAX |
|----------------------------|------------------|-----------|
| 42 V | 165 mΩ @ 10 V | 2.0 A* |

*Max current limit value is dependent on input condition.



MARKING DIAGRAM



A = Assembly Location
 Y = Year
 W = Work Week
 8402 = Specific Device Code
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|-------------------|------------------|
| NCV8402STT1G | SOT-223 (Pb-Free) | 1000/Tape & Reel |
| NCV8402STT3G | SOT-223 (Pb-Free) | 4000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCV8402

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|--------------------|------------------|
| Drain-to-Source Voltage Internally Clamped | V_{DSS} | 42 | V |
| Drain-to-Gate Voltage Internally Clamped ($R_G = 1.0\text{ M}\Omega$) | V_{DGR} | 42 | V |
| Gate-to-Source Voltage | V_{GS} | ± 14 | V |
| Continuous Drain Current | I_D | Internally Limited | |
| Power Dissipation | P_D | 1.1 1.7 8.9 | W |
| Thermal Resistance | Junction-to-Ambient Steady State (Note 1) | $R_{\theta JA}$ | 114 |
| | Junction-to-Ambient Steady State (Note 2) | $R_{\theta JA}$ | 72 |
| | Junction-to-Tab Steady State (Note 1) | $R_{\theta JT}$ | 14 |
| Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 32\text{ V}$, $V_G = 5.0\text{ V}$, $I_{PK} = 1.0\text{ A}$, $L = 300\text{ mH}$, $R_{G(ext)} = 25\ \Omega$) | E_{AS} | 150 | mJ |
| Load Dump Voltage ($V_{GS} = 0$ and 10 V , $R_I = 2.0\ \Omega$, $R_L = 9.0\ \Omega$, $t_d = 400\text{ ms}$) | V_{LD} | 87 | V |
| Operating Junction Temperature | T_J | -40 to 150 | $^\circ\text{C}$ |
| Storage Temperature | T_{stg} | -55 to 150 | $^\circ\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted onto min pad FR4 PCB, (2 oz. Cu, 0.06" thick).
2. Surface-mounted onto 2" sq. FR4 board (1" sq., 1 oz. Cu, 0.06" thick).

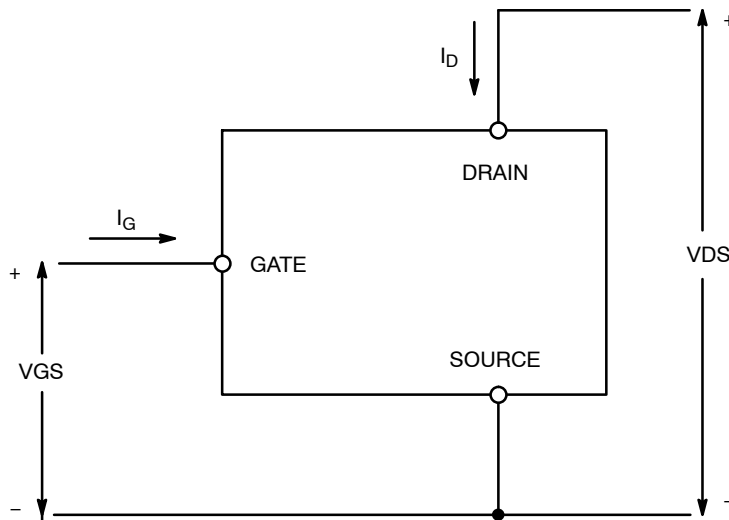


Figure 1. Voltage and Current Convention

NCV8402

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Parameter | Test Condition | Symbol | Min | Typ | Max | Unit |
|--|--|----------------------|-----|------|-----|------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-to-Source Breakdown Voltage (Note 3) | V _{GS} = 0 V, I _D = 10 mA, T _J = 25°C | V _{(BR)DSS} | 42 | 46 | 55 | V |
| | V _{GS} = 0 V, I _D = 10 mA, T _J = 150°C (Note 5) | | 40 | 45 | 55 | |
| Zero Gate Voltage Drain Current | V _{GS} = 0 V, V _{DS} = 32 V, T _J = 25°C | I _{DSS} | | 0.25 | 4.0 | μA |
| | V _{GS} = 0 V, V _{DS} = 32 V, T _J = 150°C (Note 5) | | | 1.1 | 20 | |
| Gate Input Current | V _{DS} = 0 V, V _{GS} = 5.0 V | I _{GSSF} | | 50 | 100 | μA |

ON CHARACTERISTICS (Note 3)

| | | | | | | |
|--|--|-------------------------------------|-----|-----|-----|--------|
| Gate Threshold Voltage | V _{GS} = V _{DS} , I _D = 150 μA | V _{GS(th)} | 1.3 | 1.8 | 2.2 | V |
| Gate Threshold Temperature Coefficient | | V _{GS(th)} /T _J | | 4.0 | | -mV/°C |
| Static Drain-to-Source On-Resistance | V _{GS} = 10 V, I _D = 1.7 A, T _J = 25°C | R _{DS(on)} | | 165 | 200 | mΩ |
| | V _{GS} = 10 V, I _D = 1.7 A, T _J = 150°C (Note 5) | | | 305 | 400 | |
| | V _{GS} = 5.0 V, I _D = 1.7 A, T _J = 25°C | | | 195 | 230 | |
| | V _{GS} = 5.0 V, I _D = 1.7 A, T _J = 150°C (Note 5) | | | 360 | 460 | |
| | V _{GS} = 5.0 V, I _D = 0.5 A, T _J = 25°C | | | 190 | 230 | |
| | V _{GS} = 5.0 V, I _D = 0.5 A, T _J = 150°C (Note 5) | | | 350 | 460 | |
| Source-Drain Forward On Voltage | V _{GS} = 0 V, I _S = 7.0 A | V _{SD} | | 1.0 | | V |

SWITCHING CHARACTERISTICS (Note 5)

| | | | | | | |
|---|--|-------------------------------------|--|-----|--|------|
| Turn-ON Time (10% V _{IN} to 90% I _D) | V _{GS} = 10 V, V _{DD} = 12 V I _D = 2.5 A, R _L = 4.7 Ω | t _{ON} | | 25 | | μs |
| Turn-OFF Time (90% V _{IN} to 10% I _D) | | t _{OFF} | | 120 | | |
| Slew-Rate ON (70% V _{DS} to 50% V _{DS}) | V _{GS} = 10 V, V _{DD} = 12 V, R _L = 4.7 Ω | -dV _{DS} /dt _{ON} | | 0.8 | | V/μs |
| Slew-Rate OFF (50% V _{DS} to 70% V _{DS}) | | dV _{DS} /dt _{OFF} | | 0.3 | | |

SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 4)

| | | | | | | |
|------------------------------|--|-----------------------|-----|-----|-----|----|
| Current Limit | V _{DS} = 10 V, V _{GS} = 5.0 V, T _J = 25°C | I _{LIM} | 3.7 | 4.3 | 5.0 | A |
| | V _{DS} = 10 V, V _{GS} = 5.0 V, T _J = 150°C (Note 5) | | 2.3 | 3.0 | 3.7 | |
| | V _{DS} = 10 V, V _{GS} = 10 V, T _J = 25°C | | 4.2 | 4.8 | 5.4 | |
| | V _{DS} = 10 V, V _{GS} = 10 V, T _J = 150°C (Note 5) | | 2.7 | 3.6 | 4.5 | |
| Temperature Limit (Turn-off) | V _{GS} = 5.0 V (Note 5) | T _{LIM(off)} | 150 | 175 | 200 | °C |
| Thermal Hysteresis | V _{GS} = 5.0 V | ΔT _{LIM(on)} | | 15 | | |
| Temperature Limit (Turn-off) | V _{GS} = 10 V (Note 5) | T _{LIM(off)} | 150 | 165 | 185 | |
| Thermal Hysteresis | V _{GS} = 10 V | ΔT _{LIM(on)} | | 15 | | |

GATE INPUT CHARACTERISTICS (Note 5)

| | | | | | | |
|--|--|------------------|--|------|--|----|
| Device ON Gate Input Current | V _{GS} = 5 V, I _D = 1.0 A | I _{GON} | | 50 | | μA |
| | V _{GS} = 10 V, I _D = 1.0 A | | | 400 | | |
| Current Limit Gate Input Current | V _{GS} = 5 V, V _{DS} = 10 V | I _{GCL} | | 0.05 | | mA |
| | V _{GS} = 10 V, V _{DS} = 10 V | | | 0.4 | | |
| Thermal Limit Fault Gate Input Current | V _{GS} = 5 V, V _{DS} = 10 V | I _{GTL} | | 0.15 | | mA |
| | V _{GS} = 10 V, V _{DS} = 10 V | | | 0.7 | | |

ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 5)

| | | | | | | |
|-------------------------------------|------------------------|-----|------|--|--|---|
| Electro-Static Discharge Capability | Human Body Model (HBM) | ESD | 4000 | | | V |
| | Machine Model (MM) | | 400 | | | |

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Fault conditions are viewed as beyond the normal operating range of the part.
- Not subject to production testing.

TYPICAL PERFORMANCE CURVES

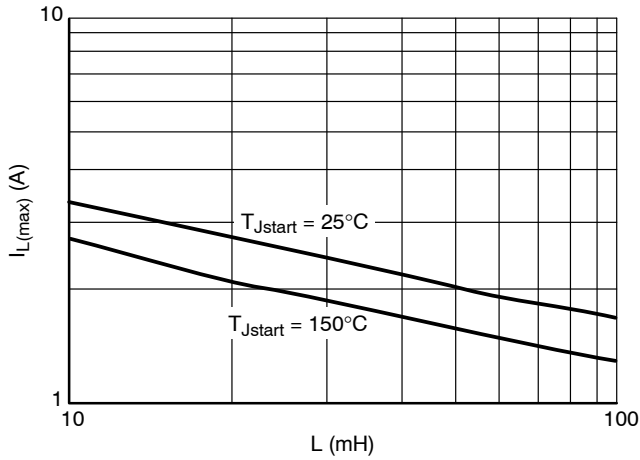


Figure 2. Single Pulse Maximum Switch-off Current vs. Load Inductance

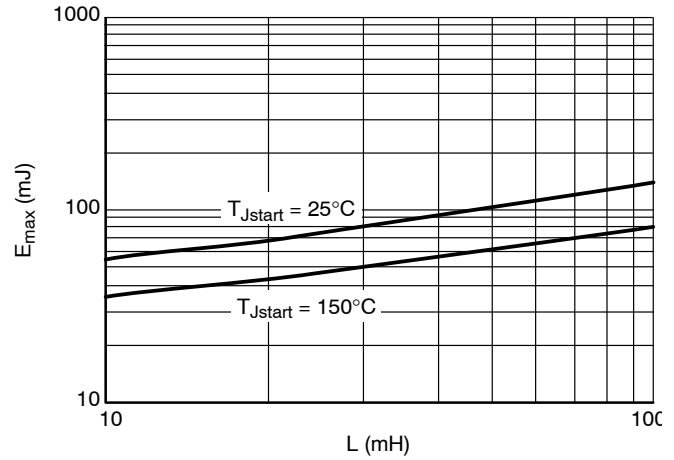


Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance

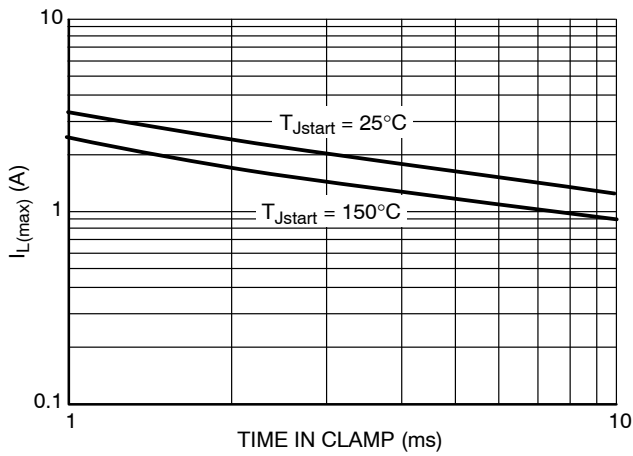


Figure 4. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp

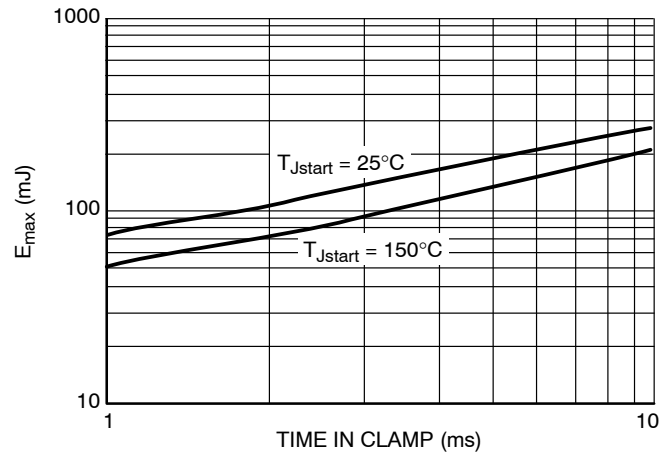


Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp

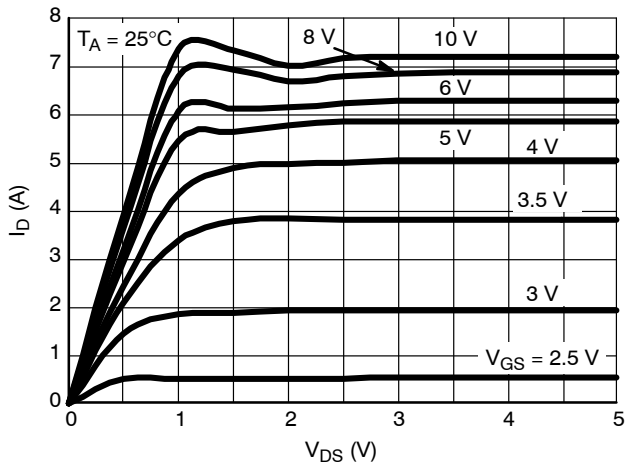


Figure 6. On-state Output Characteristics

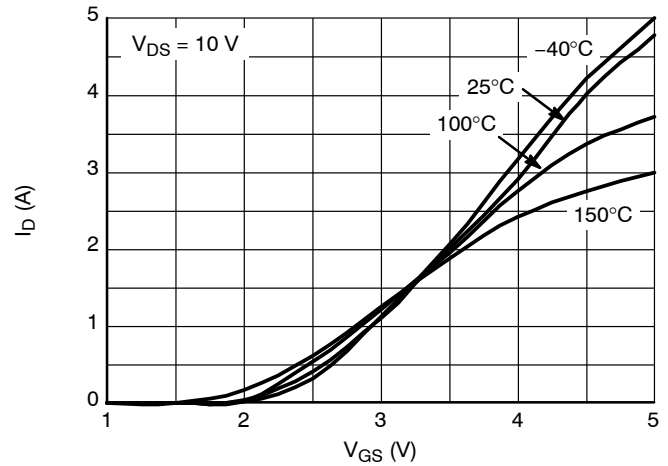


Figure 7. Transfer Characteristics

TYPICAL PERFORMANCE CURVES

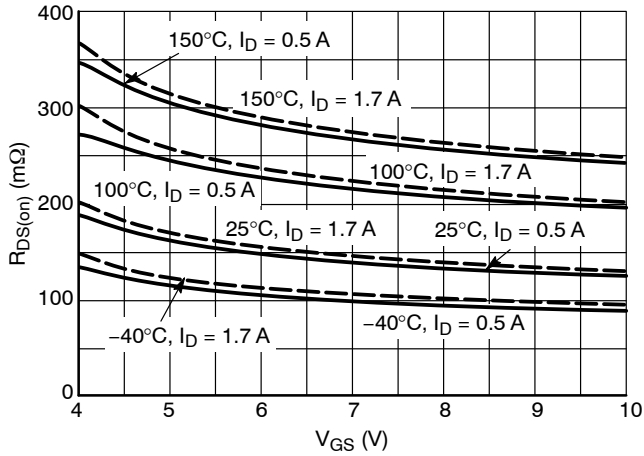


Figure 8. $R_{DS(on)}$ vs. Gate-Source Voltage

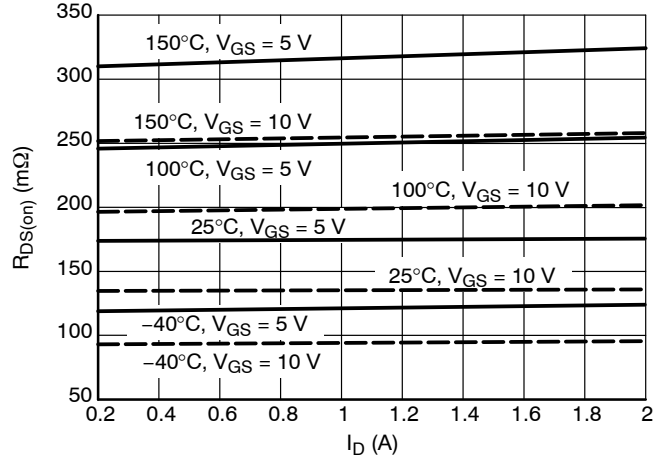


Figure 9. $R_{DS(on)}$ vs. Drain Current

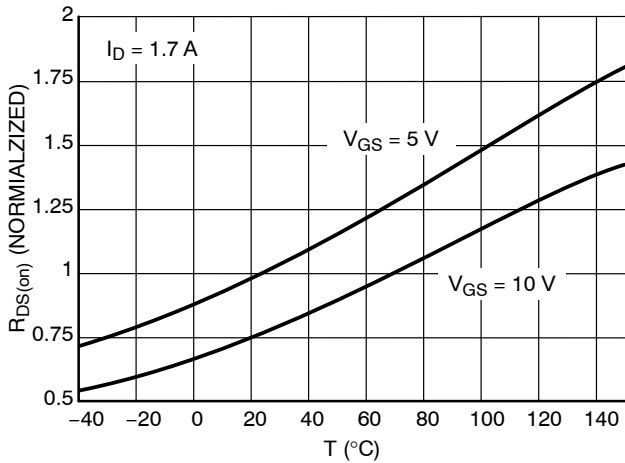


Figure 10. Normalized $R_{DS(on)}$ vs. Temperature

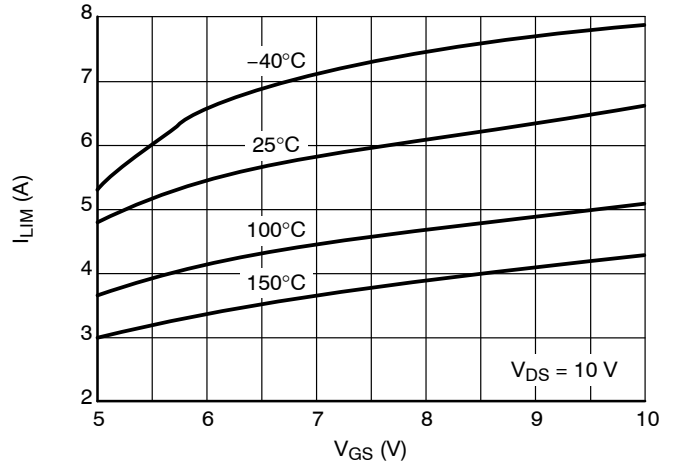


Figure 11. Current Limit vs. Gate-Source Voltage

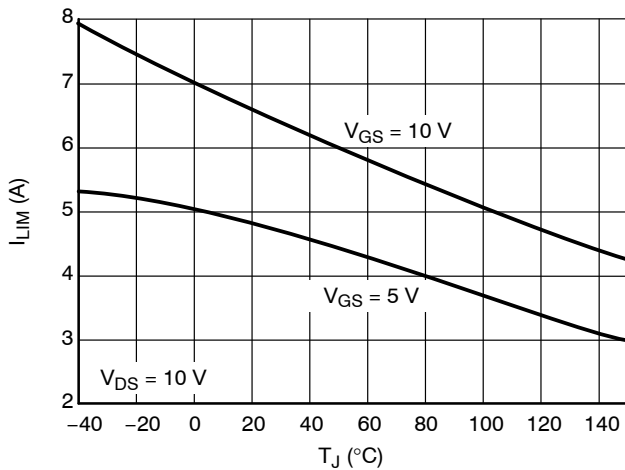


Figure 12. Current Limit vs. Junction Temperature

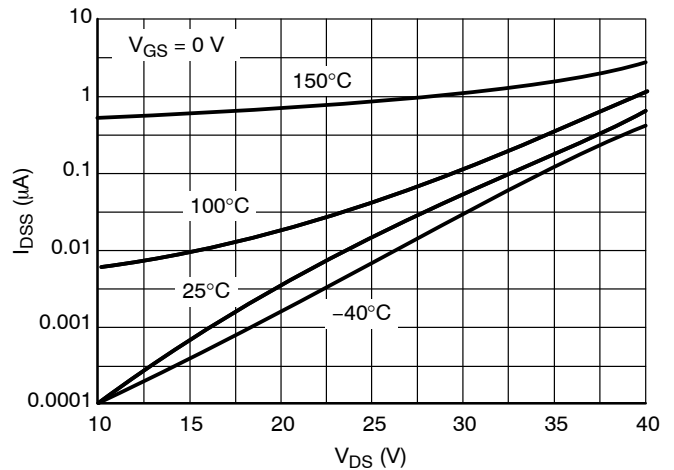


Figure 13. Drain-to-Source Leakage Current

TYPICAL PERFORMANCE CURVES

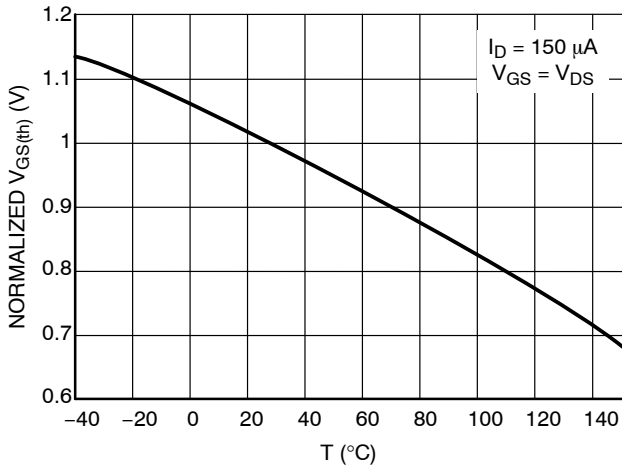


Figure 14. Normalized Threshold Voltage vs. Temperature

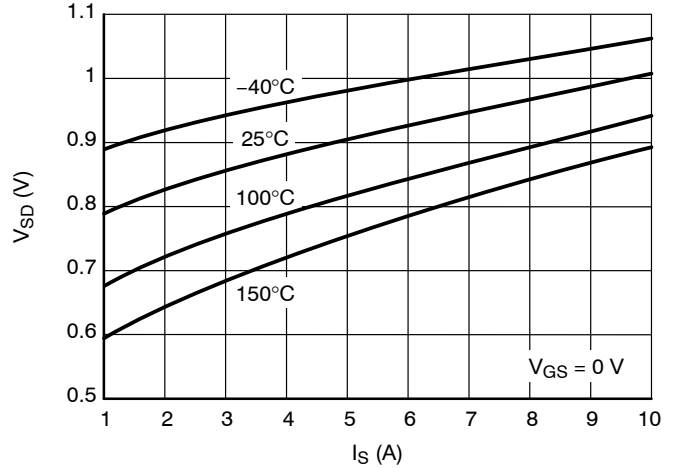


Figure 15. Source-Drain Diode Forward Characteristics

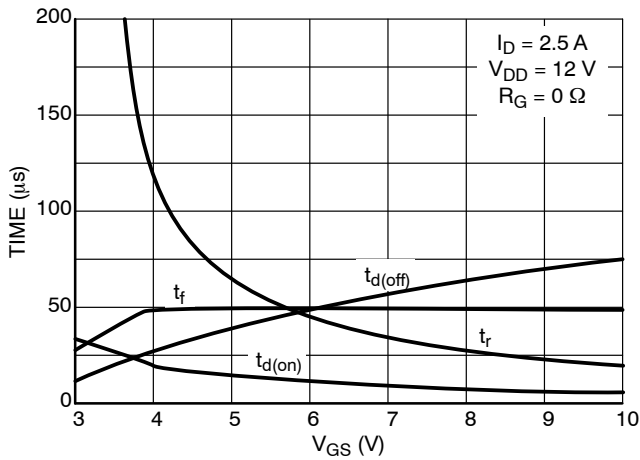


Figure 16. Resistive Load Switching Time vs. Gate-Source Voltage

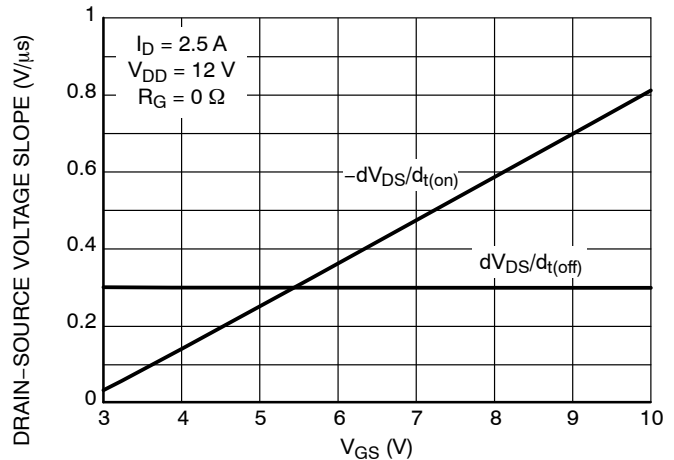


Figure 17. Resistive Load Switching Drain-Source Voltage Slope vs. Gate-Source Voltage

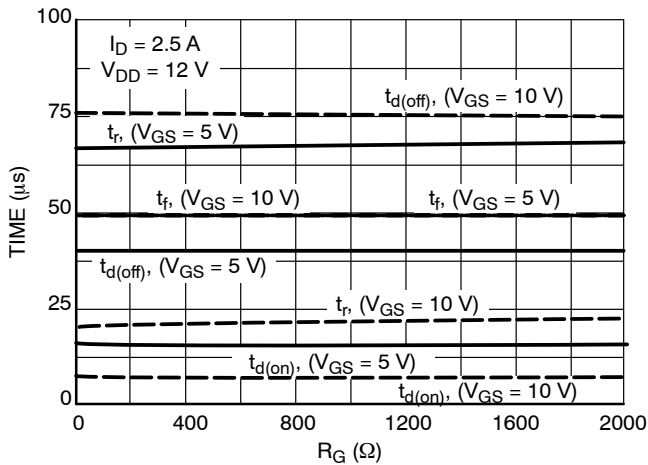


Figure 18. Resistive Load Switching Time vs. Gate Resistance

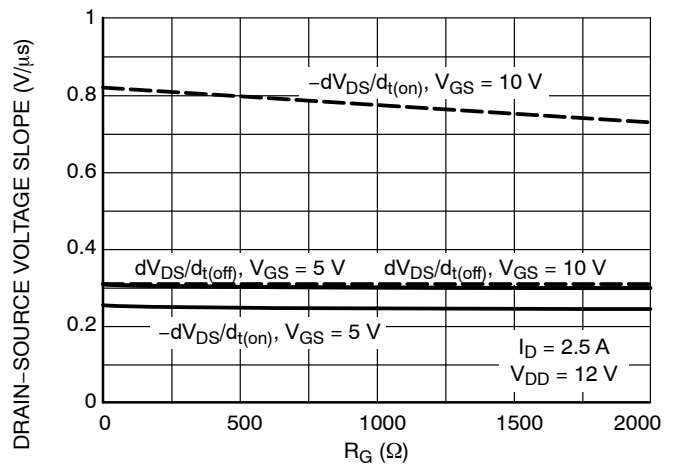


Figure 19. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

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TYPICAL PERFORMANCE CURVES

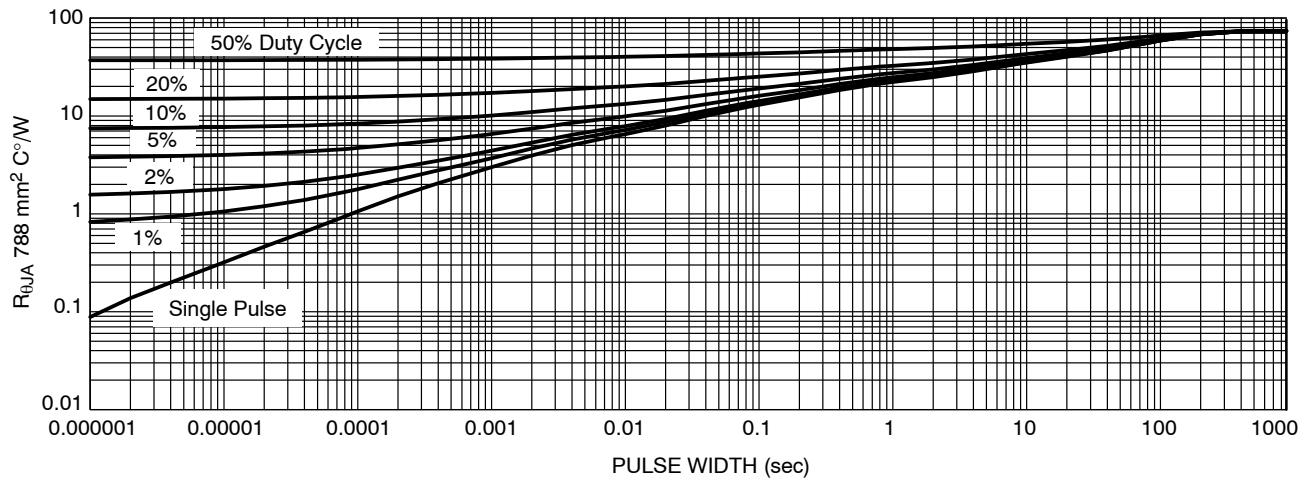


Figure 20. Transient Thermal Resistance

TEST CIRCUITS AND WAVEFORMS

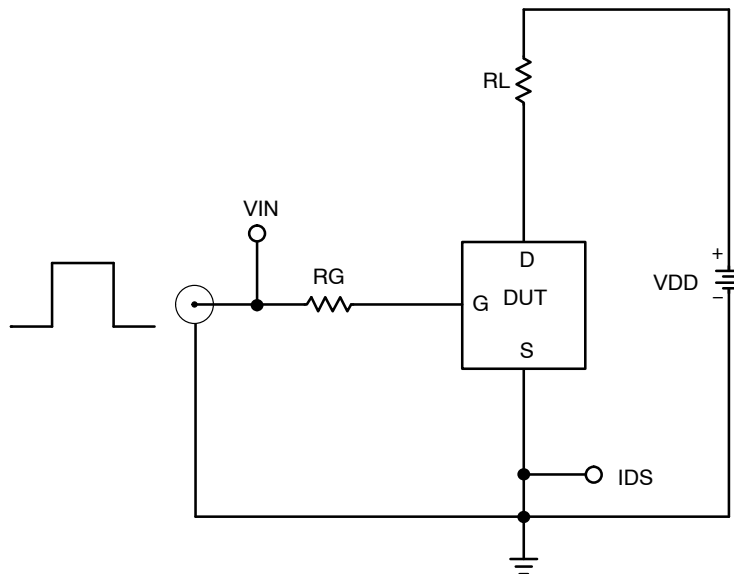


Figure 21. Resistive Load Switching Test Circuit

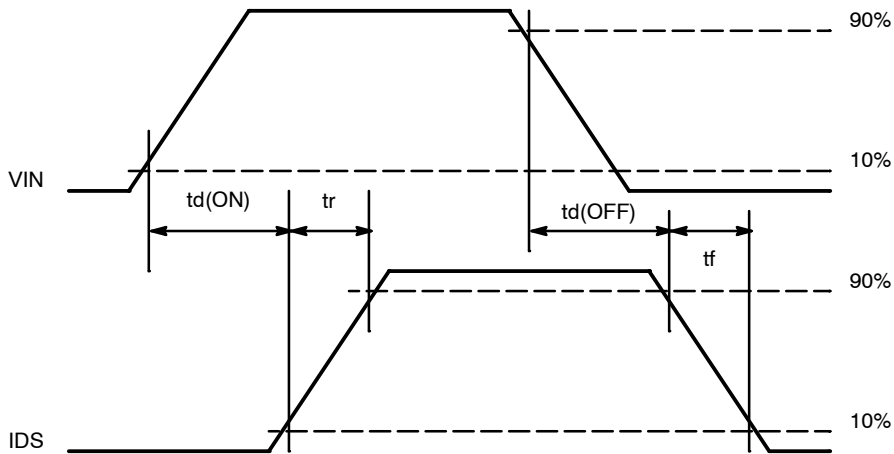


Figure 22. Resistive Load Switching Waveforms

TEST CIRCUITS AND WAVEFORMS

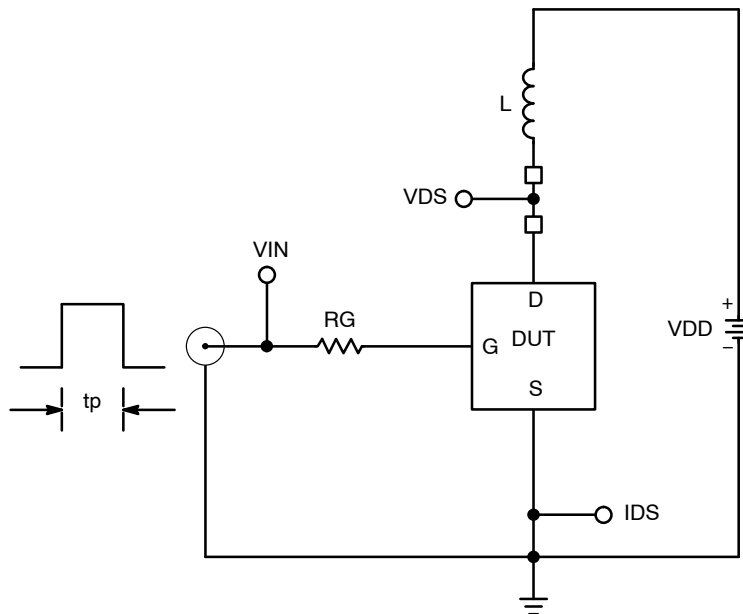


Figure 23. Inductive Load Switching Test Circuit

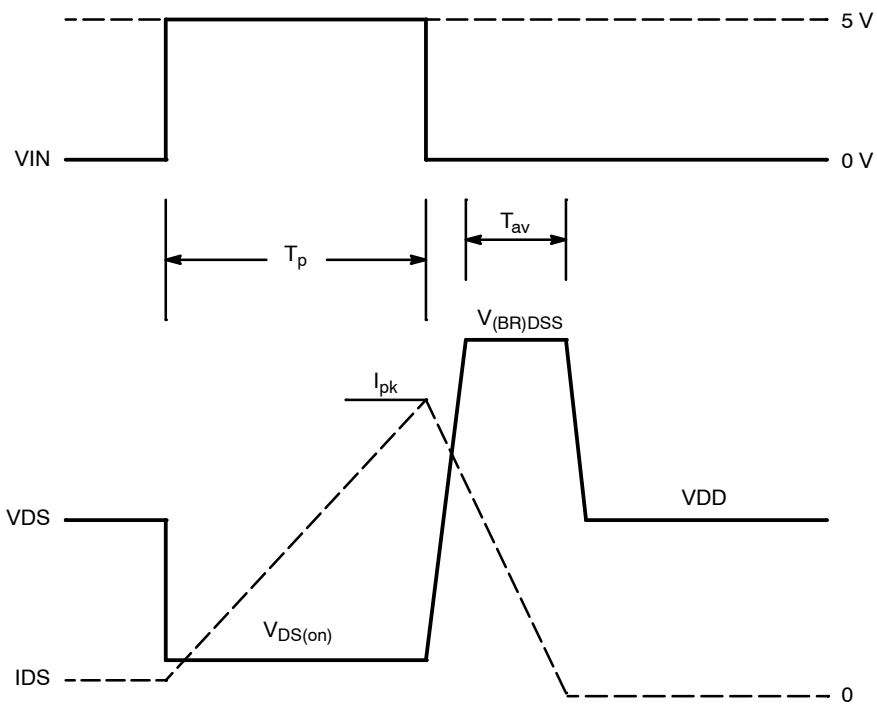
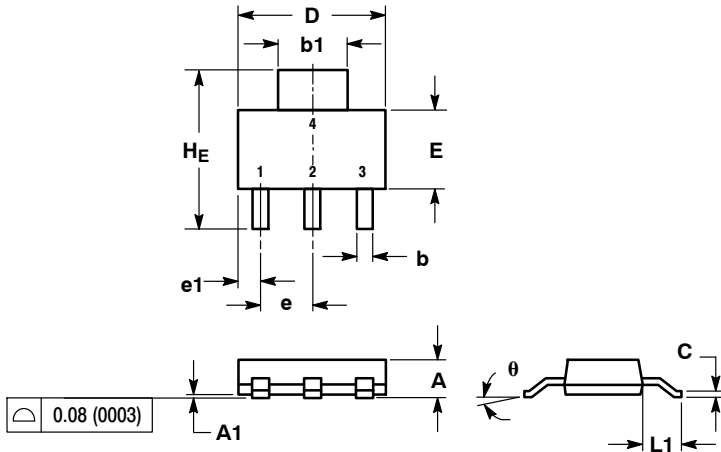


Figure 24. Inductive Load Switching Waveforms

NCV8402

PACKAGE DIMENSIONS

SOT-223 (TO-261)
CASE 318E-04
ISSUE M



NOTES:

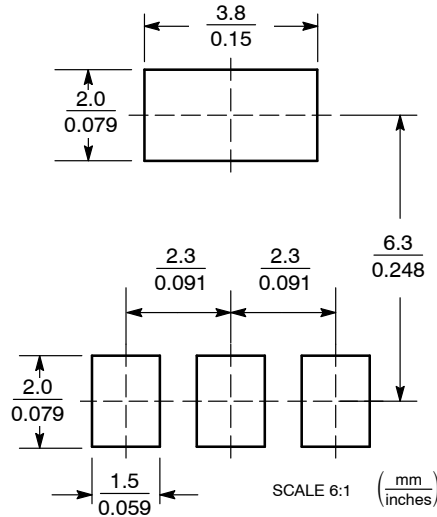
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|--------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.50 | 1.63 | 1.75 | 0.060 | 0.064 | 0.068 |
| A1 | 0.02 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.60 | 0.75 | 0.89 | 0.024 | 0.030 | 0.035 |
| b1 | 2.90 | 3.06 | 3.20 | 0.115 | 0.121 | 0.126 |
| c | 0.24 | 0.29 | 0.35 | 0.009 | 0.012 | 0.014 |
| D | 6.30 | 6.50 | 6.70 | 0.249 | 0.256 | 0.263 |
| E | 3.30 | 3.50 | 3.70 | 0.130 | 0.138 | 0.145 |
| e | 2.20 | 2.30 | 2.40 | 0.087 | 0.091 | 0.094 |
| e1 | 0.85 | 0.94 | 1.05 | 0.033 | 0.037 | 0.041 |
| L1 | 1.50 | 1.75 | 2.00 | 0.060 | 0.069 | 0.078 |
| HE | 6.70 | 7.00 | 7.30 | 0.264 | 0.276 | 0.287 |
| θ | 0° | - | 10° | 0° | - | 10° |

STYLE 3:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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